

ALU-SYS:
 NOP
 HALT
 WAIT
 RESET

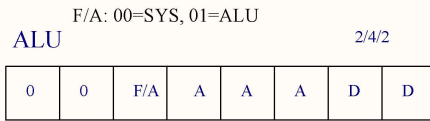
A+B, C
 ANDA, C
 NOTA, B/C
 INCB, A/C
 ROLB, A/C
 RORA, B/C

Branch:
 BRN
 BRP
 BRZ
 BRNN
 BRNP
 BRNZ
 BRO
 BRNO
 BRA

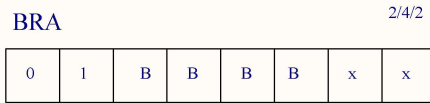
Memory:
 LDIA
 LDIB
 LDIC
 LDAA
 LDAB
 LDAC
 STAA
 STAB
 STAC
 LDDA
 Lddb
 LDDC
 STDA
 STDB
 STDC
 STAZ ? Src=null,
 dest MMA

Move Register:
 MOVAB
 MOVAC
 MOVBA
 MOVBC
 MOVCA
 MOVCB
 CLRA
 CLRB

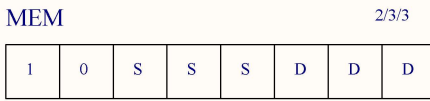
MOVAML
 MOVAMH



0000 = NOP	1000 = ADDAB	A=00
0001 = RESET	1001 = A&B	B=01
0010 = HALT	1010 = NOTA	C=10
0011 = WAIT0	1011 = INCB	
	1100 = RORA	
	1101 = ROLB	

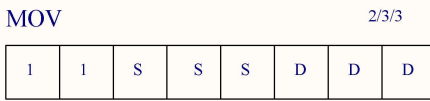


0000 = BRZ	0110 = BRO
0001 = BRP	0111 = BRNO
0010 = BRN	1000 = BRA
0011 = BRNZ	
0100 = BRNP	
0101 = BRNN	

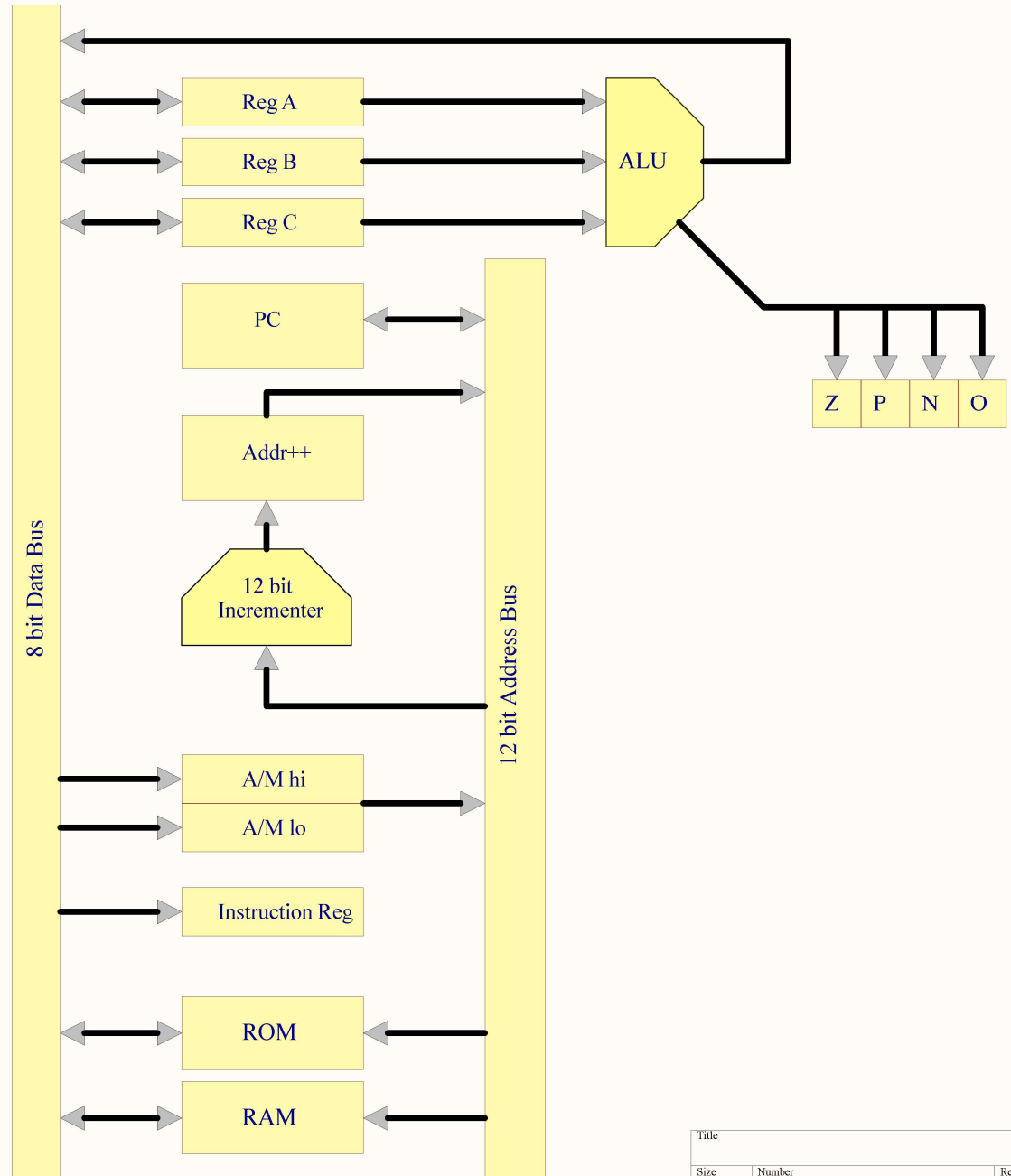


SRC	DEST
000 = A	000 = A
001 = B	001 = B
010 = C	010 = C
011 = MMI	011 = nul
100 = MMA	100 = MMA
101 = MMD	101 = MMD
111 = nul	

NB If DEST is MMA, then must be RAM
 If SRC is MMI (Immediate) then can be ROM or RAM
 If SRC is MMA (Absolute), can be ROM or RAM
 MMD refs Direct using M12 addr. reg.



A=000	A=000
B=001	B=001
C=010	C=010
M=011	MH=011
nc=100	ML=100
PC+=101	PC+=101
PC=110	PC=110
NULL=111	nc=111



Title		
Size A3	Number	Revision
Date: 10/02/2024	Sheet of	
File: C:\Users\...VerySolidArchitecture.SchDoc\Drawn By:		